AUTOZEROING CMOS LOW VOLTAGE TRANSCONDUCTANCE AMPLIFIERS

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Abstract— **Naturally simple and parallel low voltage and autozeroing current mode analog circuits Transconductance amplifiers are presented. The low voltage analog circuits are based on low voltage inverters resembling precharge digital logic. These low voltage analog circuits can be operated at supply voltages down to 240mv with rail-to-rail input and output swing. The output current of the low voltage parallel Transconductance amplifier can be quite large. The current headroom is 2.98uA and the supply voltage is 300mv. For supply voltages down to 300mv simulated data shows that the maximum clock frequency is approximately 600MHZ.**

Keywords- Differential pair-Transconductance amplifier, Autozeroing CMOS low-voltage analog-floating gate circuits, Floating-gate.

I. INTRODUCTION

The operation of analog circuits at low voltage supply becomes necessary due to semiconductor technology scaling. As supply voltages are forced down by digital constraints new circuit techniques must evolve to preserve the precision of analog functions in a mixed signal system. Low supply voltages put an upper limit on the number of gate-source voltages and saturation voltages which can be stacked. The lowest supply voltage can be obtained by biasing MOS transistor in week inversion, since this gives the smallest gate-source voltage for a given transistor. The gate oxide thickness becomes only a few nanometers and the supply voltage has to be reduced in order to ensure device reliability. An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not anticipated to decrease much below what is available today. The main reason for focusing on ultra-low supply voltages is to be able to provide analog circuitry in mixed signal ultra-low-voltage applications. Floating-gates (FG) have been proposed for Ultra-Low-Voltage (ULV) and Low Power(LP)logic. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. By using floating capacitances to the transistor gate terminals the semi-floating-gate (SFG) nodes can have a different DC level than provided by the supply voltage headroom.

Current mode analog ULV circuits based on recharge logic have been presented in the ULV recharge gates can be exploited in more general amplifier design. A basic clocked-semi-floating-gate (CSFG) autozeroing gate, Simple ULV analog circuits based on CSFG autozeroing gate, parallel ULV analog circuits are described below in different sections. In sect. II a basic clocked semi floating gate autozeroing gate is presented. Simple ULV analog circuits based on CSFG autozeroing gates are presented in sect III. Parallel ULV analog circuits are described in Sec IV and Conclusion is given in Sec V.

II. CSFG CIRCUITS

The clocked-semi-floating-gate (CSFG) transistors are shown in fig1 (a), (b). The main aim is to maintain a high current level combined with a very low supply voltage. The enhancement can be viewed as an active threshold voltage shift. The recharge transistors are controlled by a clock signals which will force the nMOS evaluate transistor gate terminal (FG) to VDD in the recharge mode, i.e. Ø=1, and the pMOS transistor gate terminal to gnd when recharging. Any input transition will affect the evaluation transistors gate voltage either by a positive or a negative charge. For very low supply voltages the CSFG biasing will not have a significant impact on the current level, and hence neither relative ON and OFF currents are large. For increasing supply voltages, up to VDD=Vt, the current level increases. For VDD≤ 0.8Vt, assuming that the floating capacitor division factor Kin>0.5 is desirable to maintain a large Transconductance. The ULV gate operation is characterized by:

Recharge: The simplified ULV inverter in recharge mode is shown in Fig1.(f). The nMOS floating-gate is recharged to $V_{offset+}$ and the pMOS floating-gate is recharged to $V_{offset-}$ while reversed biased inverter. The effective output impedance, and hence input impendence, is very low in the recharge mode.

Evaluate: The simplified ULV inverter in evaluation mode is shown in Fig1 (e). The output will be pulled

to V_{DD} if negative transition, ΔV_{in}=-V_{DD}/2 occurs and to gnd if there is a positive transition ΔV_{in}=-V_{DD}/2, applied at the input.

A. Autozeroing gates

Several techniques for compensating for process, voltage and temperature (PVT) variation have been proposed. Using a switched-capacitor (SC) biasing approach, inverter-based integrators are realized with overdrives close to the transistor threshold voltage. Chopper stabilization and autozeroing are frequently noise. Both digital analog ULV circuits are designed using autozeroing ULV inverters. The clock frequency applied must be high enough to avoid significant charge leakage during the evaluation phase. i.e. all gates simultaneously, are recharged, hence outputs are pre charged toV_{DD}/2 The precharge voltage is defined by the offset voltages v_{pre} = ($V_{offset+}$ + $V_{offset-}$)/2 due to a reverse biasing gate and simple and simple voltage division. If the evaluate transistor are matched, i.e.V_{ofset-} = V_{DD}-$V_{offset+}$ the precharge voltage can be expressed as V_{pre}≈ V_{DD}/2.Assuming that $V_{offset+}$ = V_{DD} and $V_{offset-}$ = V_{SS} = 0 V we can estimate the effect of power supply noise on the precharge voltage and accuracy of the autozeroing gate. By modelling the power supply noise as V'_{DD}=V_{DD}+ΔV1 and V'_{SS}=0V+ΔV2. We can express the precharge voltage as $Vpre = \frac{V'DD+V'SS}{2} = \frac{VDD+\Delta V1+\Delta V2}{2}$. in addition the nMOS and pMOS evaluate transistors are biased or recharged with the power noise and respectively, assuming that the precharge voltage is stable, can be expressed as $V_{gs\text{-}nMOS}$=VDD+ΔV1-ΔV2 (1)

$V_{gs\text{-}pMOS}$=-(-ΔV2+VDD+ΔV1) (2)

All ULV gates respond only to AC signal and blocked the DC level of input signals. This means the precharge level of inputs and outputs are not important for the circuit's functionality and accuracy.

III SAMPLE ANALOG ULV CIRCUITS

A. ULV current mirror

By separating the gate terminals of the transistors as shown in Fig. 2 we obtain the split gate CSFG current mirror. The gate terminals are recharged by two separate echarge transistors. More interestingly, the transistors do not share a common input capacitor. An advantage of the split gate approach is an increase in Transconductance due to less capacitance associated with the floating gates. The input capacitors may be exploited to compensate for the in accuracy

due to channel length modulation. The input Vin is swept from vdd/2=88mv to gnd. The actual precision is dependent on the matching of the capacitors. The response of the current mirror is effected by:

1. The current level or recharge current affecting the effective threshold voltage seen from the input terminal. By increasing the $V_{offset+}$ and decreasing the $V_{offset-}$accordingly we increase the current level.
2. The size of the evaluate transistors.
3. The size of the input capacitors affecting the effective transconductance.
4. The dynamic current headroom affected by the effective input voltage headroom.

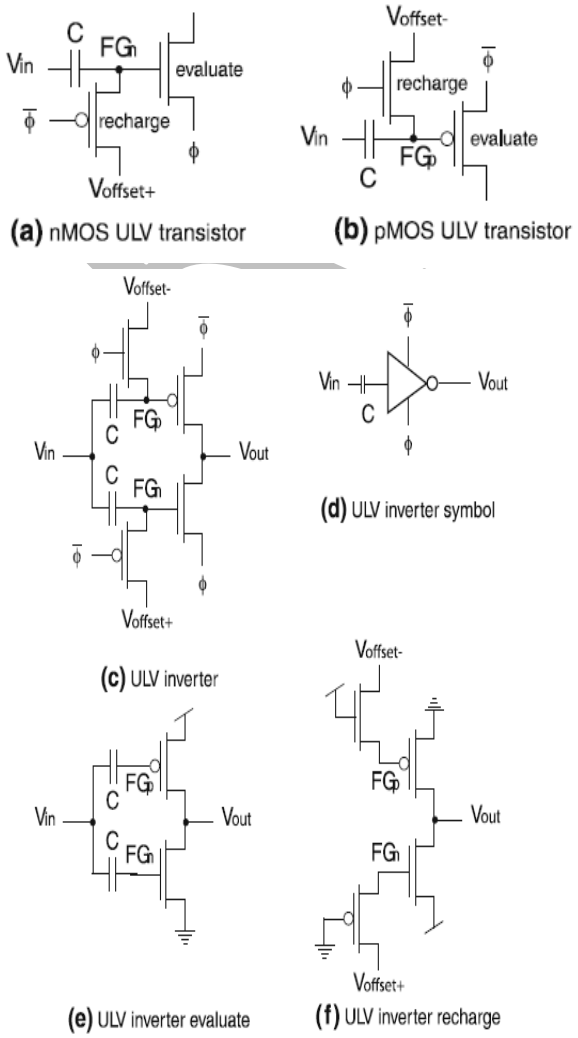


FIGURE1: a. nMOS clocked semi-floating-gate (CSFG) transistor. b pMOS clocked semi-floating-gate (CSFG) transistors. c. ULV inverter and. d. ULV inverter evaluation mode and f .ULV inverter recharge mode.

B. *ULV different pair*

By using transistors of the clock driver that provide the reference voltage we may apply two CSFG transistor in parallel powered by the same clock driver to provide a CSFG pseudo differential pair. The simple nMOS CSFG pseudo differential pairs are shown in Fig.3 (b). The clock driver provides a common reference voltage V_n to both

nMOS CSFG transistors. The clock driver (inverter) provides two alternatives current sources dependent on the clock driver input . In the case when is 0 the floating-gate (FG) nodes will be recharged to $V_{offset+}$ and the pMOS transistor of the

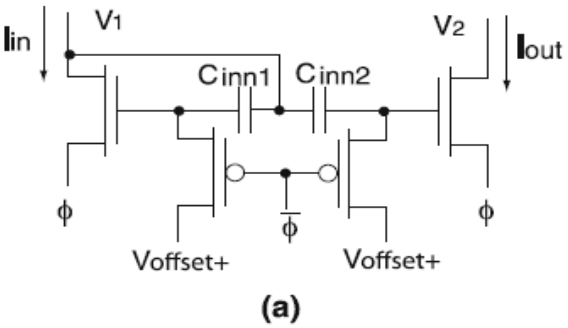


FIGURE2: a. nMOS ULV current mirror and. b nMOS ULV current mirror

Clock driver will be ON and the currents running through the evaluate transistors will be in the opposite direction than shown in the figure. The CSFG circuits resemble precharge logic characterized by a precharged or recharged phase and an evaluation phase. In the recharge phase the evaluation transistors are recharged by pulling the gate voltage to $V_{offset+}$. We may assume that the inputs are recharged to $V_{DD}/2$ and that there will be a pMOS CSFG transistor connected to each output and thereby providing a current source connected to .When the different pairs in Fig.3 (b). Is recharged the bias transistor is a pMOS transistor which is ON and thus providing a large current compared to the currents running through the nMOS evaluate transistors. Note that each nMOS evaluate transistor will have a pMOS evaluate transistor to drain the current running through the nMOS evaluate transistors. The common references Vn provide drain terminals to the two parallel nMOS evaluate transistors. The bias current is determine by the nMOS transistor of the clock driver,i.e. The gate to source voltage V_{DD} and transistor sized.

The differential current $I_{out}=I_+-I_-$ for supply voltage VDD=250mVand $V_{offset\ +}$=350mvis shown in figure 4.

C. *ULV Transconductance amplifier*

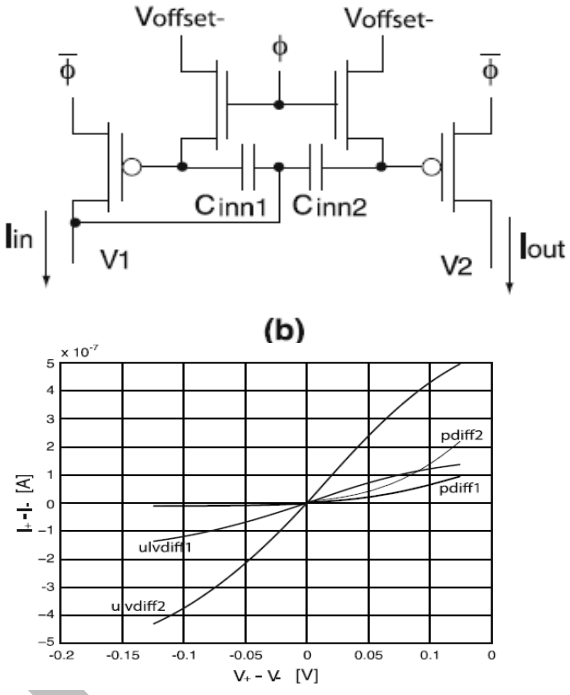


FIGURE 4:simulated response of the pseudo diff pair and a standard diff pair for a supply voltage equal to V_{DD}=250mV and $V_{offset+}$=350mV. V_ is set to $V_{DD}/2$=125mV and V+ is swept from 0v to 250v.

The nMOS ULV Transconductance amplifier is shown in Fig.5. The bias current is determined by the nMOS transistor of the clock driver, i.e. the gate to source voltage V_{DD} and transistor size. The bias transistor will have a gate to source voltage equal to V_{DD}. Due to the offset imposed on floating gate the two transistors of the pseudo differential pair may have a gate to source voltage higher than V_{DD}. In order for the bias transistor to pull the amount of current running through the pseudo differential pair we increase with the bias transistor.

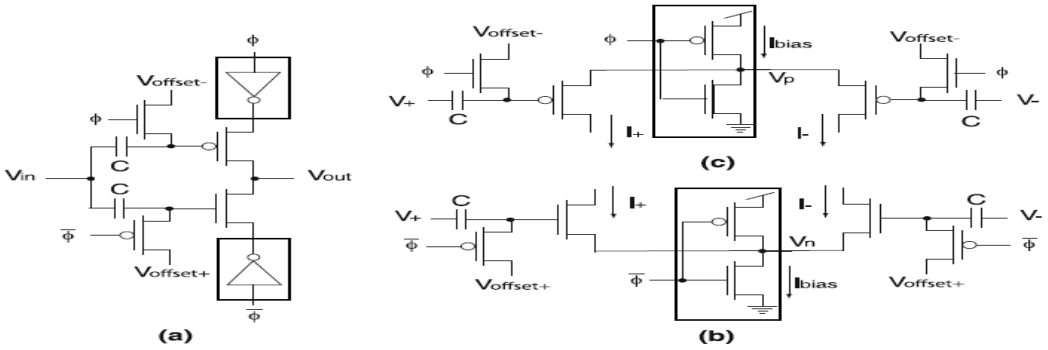


FIGURE 3: a. ULV inverter with clock driver's b. nMOS ULV differential pair and c. pMOS ULV differential pair.

The requirement for the diff pair to operate is that the bias transistor is in saturated, i.e. velocity saturated, region. If bias transistor is sinking too much current compared to the nMOS diff pair the common source will be pulled too close to leaving the bias transistor in the triode region. If the bias transistor is operating in the triode region an increase in one of the inputs will yield an exponential or quadratic increase in current. If an input decreases, the output current will be affected significantly due to a virtual ground at the common source. In order to keep the bias transistor in the saturation we need to have a common source V_n above the saturation voltage. In recharge mode the ULV amplifier the output V_{out} and the internal node V_a are autozeroed. The autozero value depends on the evaluate transistors and the offset voltages applied. Both Va and V_{out} will be forced to a level close to $V_{DD}/2$. The accuracy or linearity of the amplifier is not dependent on the precision of the autozero levels. The transconductance of the evaluate transistors are more important for the response of the amplifier.

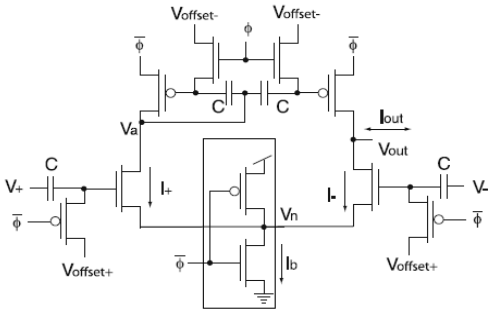


FIGURE 5: nMOS ULV Transconductance amplifier.

IV. PARALLEL ULV CURRENT CIRCUITS

A. Parallel ULV current mirror

The simulated response of the simple current mirror shown in Fig.2 will be restricted by the input and output current level and the polarity of the input current. The response of the parallel ULV current mirror shown in Fig.6 is less sensitive to the voltage levels of the input and output. We may examine the circuit response to a recharge operation. During recharge the nMOS floating-gate voltages are fixed to $V_{offset+}$ while the pMOS floating gate voltages are equal to $V_{offset-}$, the node voltages at *in* and *out* are $V_{DD}/2$ and the current are equalized, i.e.$I_{n1}=I_{n2}=-I_{p1}=-I_{p2}$furthermore the input and output currents are assumed to be 0. Assume that the input current increases compared to I_r which is the current running through the evaluate transistors in the evaluation mode with no input changes applied. This will lead to an increased voltage at the input *in* i.e. assuming a pMOS transistor feeding a positive current in to *in* As a result the currents I_{n1} and I_{n2}will increase and I_{p1} andI_{p2}will be reduced accordingly. We may express the change in transistor currents as

$$\Delta I_{n1}-\Delta I_{p1}=\Delta I_{in}$$

$$\Delta I_{n1}=\Delta I_{in}+\Delta I_{p1}$$

$$\Delta I_{n2}=\Delta I_{in}+\Delta I_{p2} \quad (3)$$

$$\Delta I_{n2}-\Delta I_{p2}=\Delta I_{in}$$

$$\Delta I_{out}=\Delta I_{in}$$

The input stage will act as a current to voltage converter and the output stage will act as a voltage to current converter. The change in input and output currents can be negative or positive. The actual input and output currents can be expressed as

$$I_{in}=I_r+\Delta I_{in}$$
$$I_{out}=I_r+\Delta I_{out} \quad (4)$$
$$I_{out}=I_{in}$$

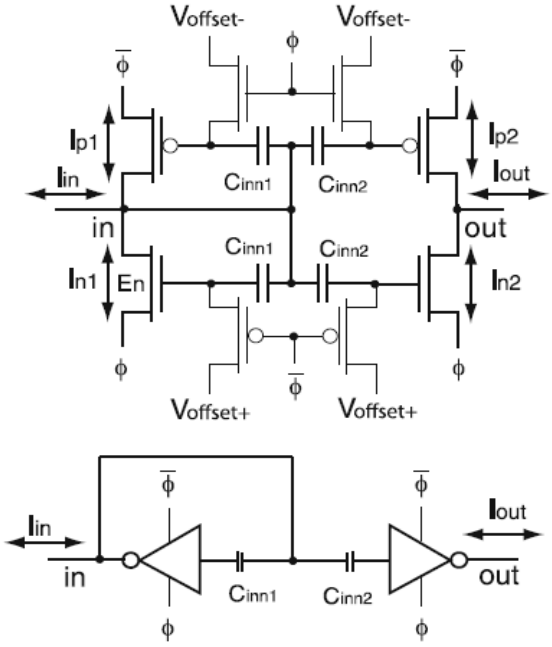


FIGURE 6: parallel ULV current mirror. Simplified representation using Inverter and ULV inverter is shown

The input current in will pull the input terminal towards V_{DD} or V_{ss} depending on the polarity of the current. A negative current will pull the input terminal down and a positive input current will pull the input up. The input current will be matched by a current provided by the inverter in the I and V converter. The I to V converter will generate an input voltage to drain the actual input current. If the input current is equal to the recharge current I_r the circuit is stable and the input voltage is equal to $V_{DD}/2$. The drained input current will be available at the output due to a corresponding change in the floating gate of the inverter producing the output current. If the capacitors C_{inn1} and C_{inn2} are equal the voltage change at the semi floating gates and hence the output

currents will match the current running through the inverter in the I to V converter which is equal to the input current. The accuracy of the current mirror is determined by mis matches of the transistors and capacitors. The transistor mismatches will affect the precharge value. We may expect that the pre charge voltage will adapt to the relative mismatch of the transistor is strong compared to a standard transistor the node driven by the transistor may pre charge at a higher level than $V_{DD}/2$ and the node voltage will be pulled lower than $V_{DD}/2$ the circuits enter the evaluate mode. The change in node voltage will affect the driving circuit through a parasitic node to floating gate parasitic capacitance. The accuracy of the capacitors may be increased by using larger poly-poly capacitors. The input V_{inn} and the output Vout are inversed with a DC value equal to $V_{DD}/2$. The frequency of the input signal is 10MHz and the recharge frequency is 25MHz.

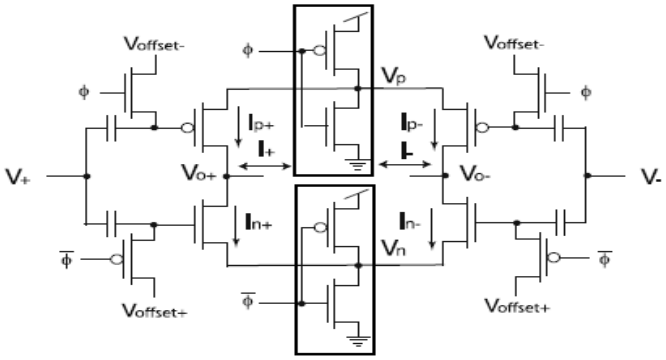


FIGURE 7: simulated response of the symmetrical current mirror.

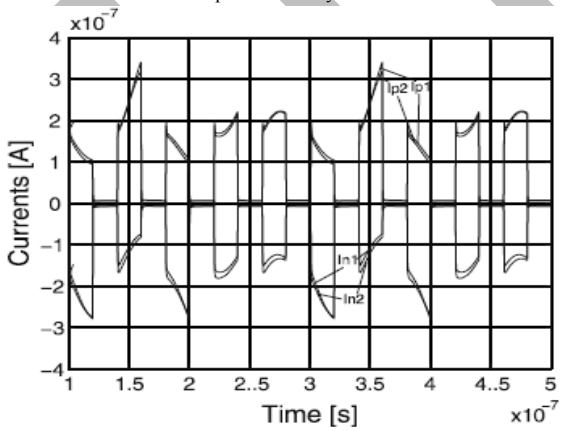


FIGURE 8: Parallel ULV pseudo differential pair.

The output current of the symmetrical diff pair is defined as

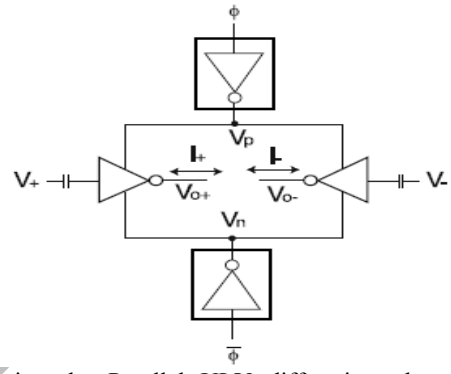
$I_{out}= (I_{p+}-I_{n+})-(I_{p-}-I_{n-})$

$=-I_{+}-I_{-}$

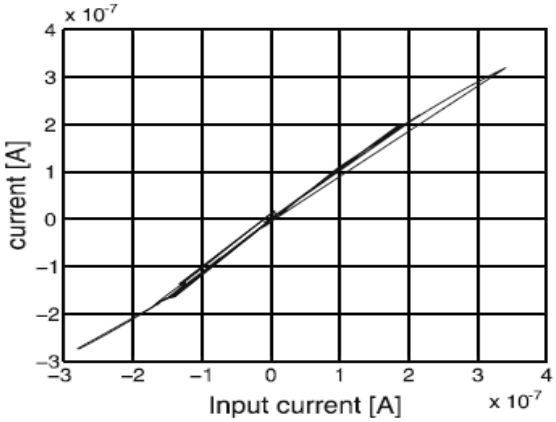
Assuming matched transistors both outputs will be precharged to $V_{DD}/2$ due to the voltage divider configuration and low impedance output. If one input, for example V_{+} increases and the other input is stable, the current I_{n+} will increased and I_{p-} will decrease and the current will be drained from the negative output and V_{out-} will be reduced. Furthermore, the pseudo diff pair will adapt and a positive current will raise V_{out+}. The output current of the ULV diff pair is shown in fig.8, where the supply voltage is 200mV and the offset voltages are 250mV and 50mV. V_ is equal to 100mV and V+ is swept from 0v to 200mV.

The output current of the ULV diff pair is shown in fig.9, where the supply voltage is 300mV and $V_{offset+}$=350mv and V_{offset}=-50mv, V- is swept from 0 to 300mV and W_{bias}=50µm The output current of the ULV diff pair is shown in Fig.10, where the supply voltage is 300mV and the offset voltages are $V_{offset+}$=350mv and $V_{offset-}$=-50mv, V- is swept from 0 to 300mVand V= is swept from 0v to 300mv, and W_{bias}=50µm

B. Parallel ULV transconductance amplifier



By combining the Parallel ULV diff pair and a symmetrical ULV current mirror we obtain the



parallel ULV transconductance amplifier as shown in fig.12. The standard inverters are proving the degraded supply voltage V_p and V_n used to power the symmetrical differential pair. As shown the proposed transconductance amplifier can be drawn using inverters and floating capacitors. The timing response is not dependent on the DC level or amplitude of the differential input. Furthermore, rail to rail input signals and output signal can be used. The clock frequency is limited by

1. The clock frequency must be high enough to avoid the impact of floating-gate leakage; hence a frequency above 1MHz is satisfactory.

2. The clock frequency cannot excess the fundamental timing response of the circuit. For VDD=$V_{offest+}$=300mV preliminary simulated data show that the maximum clock frequency is approximately 600 MHz's.

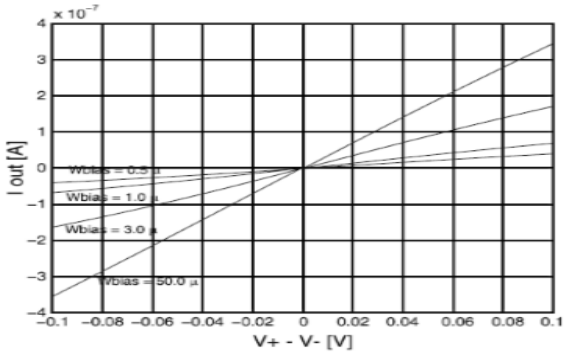


Figure 9. Simulated output currents of the symmetrical ULV diff pair

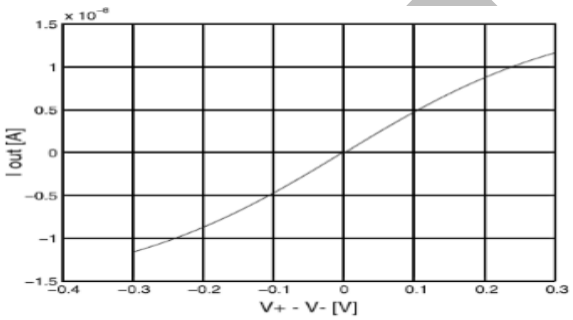


Figure 10. Simulated output currents of the symmetrical ULV diff pair V_{dd}=300 mv and W_{bias}=0.5µm

Furthermore, if a dc signal is applied to the input the output will eventually be driven to VDD/2 because the amplifier will be initiated in each clock period. Any input signal frequency increasing the lower clock frequency limit will affect the output current by a change from the initial state according to a change of the differential input. This can be expressed as

$\Delta I_{out}=I_r+F(\Delta V+-\Delta V)$

Where I_r is the current after recharge and F is a tanh shaped function determined by the pseudo differential pair.

If the clock frequency exceeds the input signal frequency the output current will be limited determined by the maximum differential voltage provided in the evaluation phase. The input signal amplitude is not restricted to the supply voltage used for the amplifier. However, if high amplitude inputs signal are used the clock frequency should be larger than the input frequency in order to reduce the output current and maintain accuracy by securing that the transistor are operate din the saturation region .

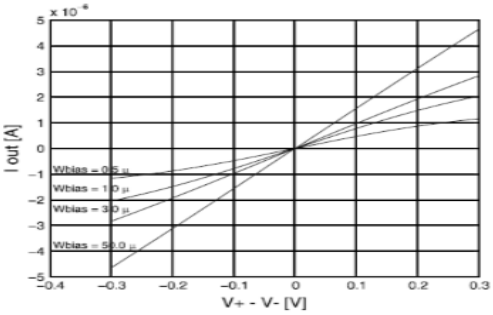


Figure11. Simulated output currents of the parallel ULV diff pair Vdd=300mv.

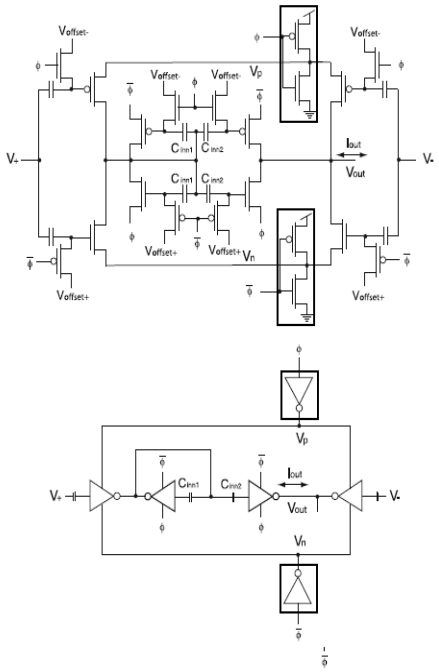


Figure 12: Parallel ULV transconductance amplifier.

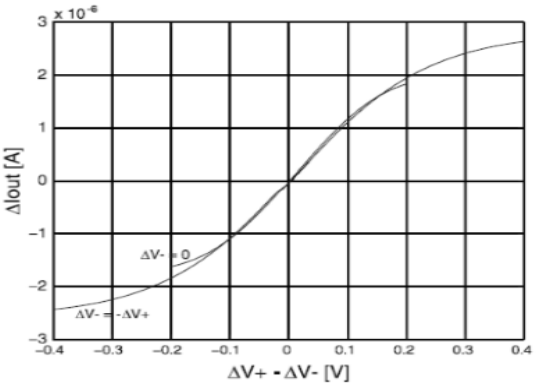


Figure 13.Simulated output currents of the parallel ULV transconductance amplifier. Vdd=300mv. The output current is not determined by the dc level of the input.

V. CONCLUSION

Fully Parallel and auto zeroing analog circuits for low supply voltages have been presented. The floating capacitors of the Parallel current mirror are draw to compensate for the output resistance. Low-voltage analog circuits can be operated at supply voltages down to 240mV with rail-to-rail input and output swing. The output current of the low-voltage parallel transconductance amplifier quite large due to a current boost technique. The different supply voltages are used to show that the different supply voltages are used to show that the different sub circuit can operate at extremely low supply voltages. The current mirror do not use a biasing transistor provided by a clock driver and may therefore operate at lower supply voltages than the diff pair and the amplifier.

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